REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application, indicating that claim 8 is allowable, and indicating that claims 19 and 30 contain allowable subject matter.

I. Disposition of Claims

Claims 1-33 are pending in the present application. Claims 1, 12, 19, 23, and 30 have been amended.

II. Claim Amendments

Independent claims 1, 12, and 23 of the present application have been amended to include the limitations of obtaining a representative power supply waveform having noise and digitizing the representative power supply waveform having noise, where the digitized representative power supply waveform having noise into then input to a simulation of a phase locked loop. Further, independent claims 1, 12, and 23 of the present application have been amended to remove the limitation "wherein the noise is incident to supplying power to the phase locked loop." No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 5a of the present application.

Dependent claims 19 and 30 of the present application have been rewritten in independent form including all of the limitations of the base and any intervening claims as pending immediately prior to this reply. No new matter has been added by way of

these amendments. Accordingly, amended claims 19 and 30 of the present application are now allowable.

III. Allowed Claim

Claim 8 of the present application has been allowed. Applicant thanks the Examiner for carefully reviewing and allowing claim 8 of the present application.

IV. Rejection(s) Under 35 U.S.C § 102

Claims 1-7, 9-18, 20-29, and 31-33 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by Jenkins et al. ("Measuring Jitter and Phase Error in Microprocessor Phase-Locked Loops," Keith A. Jenkins and James P. Eckhardt, IEEE Design and Test of Computers, April – June 2000, pages 86-93). For the reasons set forth below, this rejection is respectively traversed.

The present invention is directed to a technique for estimating/determining jitter of a phase locked loop based on a simulation of the phase locked loop using a representative power supply waveform. *See* Specification, paragraph [0025]. Amended independent claims 1, 12, and 23 of the present application require at least (1) obtaining a representative power supply waveform having noise (*e.g.*, **172** in Figure 5a of the present application), (2) digitizing the representative power supply waveform having noise (*e.g.*, **174** in Figure 5a of the present application; Specification, paragraph [0028]), (3) and inputting the digitized representative power supply waveform having noise into a simulation of a phase locked loop (*e.g.*, Figure 7 of the present application).

Jenkins et al., in contrast to the present invention, fails to teach the arrangement of

the present invention as recited in amended independent claims 1, 12, and 23 of the present application. For example, Jenkins et al. does not disclose, or otherwise teach, digitizing the representative power supply waveform having noise as required by amended independent claims 1, 12, and 23 of the present application. As shown in Figure 5 of Jenkins et al., the noise generator circuit, which "introduces noise on the PLL power supply" (*see* Jenkins et al., page 89, lines 21 – 27), uses an "external resistor (R_{ext}) [that] causes a change in the *analog* supply-voltage level." Jenkins et al., page 89, lines 27 – 31 (emphasis added). As shown by the circuit schematic shown in Figure 5 of Jenkins et al. and the block diagram shown in Figure 6 of Jenkins et al., this analog supply-voltage level is propagated by the V_{DDA} pin of the noise generator circuit directly to an input of the PLL. There is no digitization of the supply voltage before it is input to the PLL. Further, Jenkins et al. specifically refers to the power supply voltage V_{DDA}, which serves as the input to the PLL (Figure 6 in Jenkins et al.), as an "analog voltage." *See, e.g.*, Jenkins et al., page 91, line 33; Jenkins et al., page 91, lines 40; Figure 7 of Jenkins et al.

On the other hand, as described in the present application and claimed in amended independent claims 1, 12, and 23 of the present application, the representative power supply waveform having noise is digitized before serving as an input to a PLL simulation. *See* Specification, paragraph [0028]. Digitization leads to more accurate simulation relative to cases in which, for example, analog or square waveforms are input to the PLL simulation. *See* Specification, paragraph [0028]. However, as discussed above, Jenkins et al. fails to disclose, either explicitly or impliedly, the digitization of the representative power supply waveform having noise for inputting to a PLL simulation as

required by amended independent claims 1, 12, and 23 of the present application.

In view of the above, Jenkins et al. fail to show or suggest the present invention as recited in amended independent claims 1, 12, and 23 of the present application. Thus, amended independent claims 1, 12, and 23 are patentable over Jenkins et al. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

V. Conclusion

The above amendments and remarks are believed to require no further prior art search. Also, Applicant believes this reply to be responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Because the amendments and remarks simplify the issues for allowance or appeal, and do not constitute new matter, entry and consideration thereof is respectfully requested. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.170001;P7188).

Respectfully submitted,

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